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an input port of one of the modules and a respective output port of the one module wherein each KxK interconnect module includes a plurality of LxL passive interconnect modules, L<K.--

--75. An interconnect as in claim 74 with $\frac{K}{L}$ groups of signal carriers coupled to respective LxL modules.--

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REMARKS

This Amendment is in response to the Office Action mailed October 15, 2002 with a three-month response period. By this Amendment, a number of the claims have been amended so as to more clearly set forth the present invention. Objected-to claim 66 has been rewritten in independent form. Several new claims have been added. For the following reasons, the pending claims are all allowable over the prior art of record.

A signal interconnect network which embodies the present invention provides a systematic and modular solution to the difficult and expensive problem of having to route multiple electrical or optical signals between a plurality of ports in an electrical or optical switch or, in a module in such switches. As illustrated in Fig. 1 of the present application, known interconnect fabrics require N^2 connections to couple N inputs to N outputs. These fabrics become very expensive and difficult to manufacture as N gets larger and larger.

Interconnect networks in accordance with the present invention solve this problem by providing one or a few standardized, passive interconnect modules. Such modules are efficient to manufacture, to test and to assemble into larger interconnect structures of arbitrary sizes while still retaining all of the benefits of the basic modular interconnect structure. Such structures route optical or electrical signals, via dedicated, not multiplexed, signal paths, between selected inputs and outputs. Hence, an optical or electrical signal input at one port of a network as claimed, will be transmitted, without processing to the corresponding output of the network.

Modules in accordance with the present invention interconnect inputs and outputs by providing a plurality of dedicated signal paths. Signals are not combined or demultiplexed as they traverse these modules. Larger fabrics can be formed of recursively connected multi-level modules by interconnecting pluralities of relatively small base modules to form intermediate size

fabric modules and then interconnecting a plurality of intermediate size modules to form a larger fabric.

In this regard, Fig. 2A of the application illustrates an exemplary KxK module, where K = 4 which supports K^2 or 16 separate, passive signal carriers or paths, which could be optical or electrical, between the K^2 inputs and outputs. Modular interconnect fabrics in accordance herewith provide K^2 separate signal carrying conduits, which could be optical fibers or electrical wires, for each of the K^2 signals. Signal processing precedes or succeeds the modular interconnect structures of the present invention.

Suemura et al have solved a different problem in implementing an optical network and have not in any way addressed modular interconnect networks as claimed. The teaching of Suemura et al, as illustrated I Figs. 3, 5, 8 and 11 for example, is to simply make the necessary interconnections of optical fibers without a module approach as claimed. Suemura et al teach away from the claimed structures. Suemura also incorporates optical processing into those structures which is unlike the claimed interconnect structures.

On page 3 of the Office Action, in rejecting claim 41 the Examiner identified signal modules 123 as corresponding to the claimed interconnect module. Fig. 9 illustrates the structure of the various modules 123 of Fig. 8. Each such module incorporates an optical splitter 127(i) as in Fig. 7 which provides multiple outputs and is coupled to an optical multiplexer 129(i) as in Fig. 6. As is illustrated in Fig. 9, the modules 123 carry out signal processing with the output signals each representing a multiplexed composite signal λ 0, λ 1, λ 2 and λ 3. Unlike the outputs, each of the inputs corresponds to a singular frequency λ 0 or λ 1 or λ 2 or λ 3.

Suemura et al thus teach signal processing and combining in the single modules 123. The input signals such λ 0, λ 1, λ 2 and λ 3 available individually on the input side of the module are not available individually but are included in composite signals on the output side of the respective modules. Hence, Suemura teaches optical signal processing via splitter 111 and multiplexer 99 (Fig. 7, 6 thereof) which is unlike the claimed invention. Additionally, Suemura et al combines the signals onto common optical links which is also unlike the claimed invention.

In rejecting claim 41, reference was also made to Fig. 11 and element 75, a cross-bar switch as in Fig. 3. That circuitry does not address modular interconnect modules as claimed. Increasing the number of inputs and outputs results in an increasing complexity of the internal A

connections. Suemora et al do not address this problem. This is the problem sovled on a modular basis by the present invention.

Suemura et al never recognize, teach nor suggest the use of recursively derivable, passive interconnect fabrics, which only provide an interconnect function, based on the use of multiple pluralities of substantially identical interconnect modules as claimed. In this regard, in rejecting claim 58, the Examiner has asserted that:

> "Suemura further teaches wherein each of the KxK signal interconnect module (see fig. 8, item 123) comprises a plurality of substantially identical LxL interconnect modules (shown in Fig. 11, items $123_{0\text{-}3}$ and $75_{0\text{-}3}$)."

As noted above, the structure 123 is unlike the claimed KxK modules. The reference to Fig. 11 does not cure the deficiencies in the disclosure or suggestions put forth by element 123, see Fig. 9 of Suemura. Further, the Examiner's attempted reading of the structure of claim 58 on Fig. 11 simply is inconsistent with the wording of claim 58 and does not make obvious the wording thereof. In this regard, Fig. 11 illustrates a plurality of modules 123 having the same structure which was discussed previously.

If the claimed interconnect module in the Examiner's reading of claim 58 corresponds to item 123 (°) ... 123 (3) then those same modules cannot correspond to the "plurality of substantially identical LxL interconnect modules (shown in Fig. 11, items $123_{0\text{-}3}$ and $75_{0\text{-}3}$)." The reference to items $123_{0\text{-}3}$ and $75_{0\text{-}3}$ in this reading of the rejection of claim 58 is inadequate to make claim 58 obvious wherein claim 58 requires:

> "wherein each of the KxK signal interconnect modules comprises a plurality of substantially identical LxL interconnect modules where L less than K."

The structure recited above in combination with the limitations of claim 41 defines a multi-level modular structure where the KxK modules each incorporate a plurality of LxL modules. The claimed structure is simply not present in and not suggested by Suemura et al which does not address a modular interconnect structures of any sort.

Similar comments apply to the rejection of claim 59.

The rejection of claim 63 is also similarly defective. The Examiner has again asserted that the element 123 corresponds to the claimed KxK module. In claim 63 "each KxK module comprises a body portion which includes a plurality of LxL signal coupling networks with L<K." Items 123 and 75 of Fig. 11 unlike the Examiner's assertion on page 5 of the Office Action do not correspond to the above-noted limitation pertaining to "a plurality of LxL signal coupling networks" which as claimed make up each KxK module. The wording on page 5 of the Office Action rejecting claim 63 simply does not address the claimed structure.

If the elements 123 correspond to claimed KxK modules as asserted by the Examiner, then the claimed respective body portion which includes a plurality of LxL signal coupling networks represents a structure which is incorporated into each claimed KxK module. The elements 75(i) are not incorporated into the elements 123(i) as claimed. Rather, they are coupled to respective separate, upstream elements 123(i) and receive output signals previously processed by respective elements 123(i). The wording of the rejection simply does not address the claimed structure.

Fig. 11 of Suemura et al illustrates an interconnect structure between a plurality of elements 123 and a plurality of separate elements 75. In addition, the elements 75 of Fig. 11 as illustrated in Fig. 3 of Suemura et al include both splitters and combiner elements which carry out signal processing first splitting signals into multiple copies and then combining various signals together which represents structures and signal processing unlike the claimed apparatus. In summary, each of the elements 123(i) and 75(i) carry out signal processing unlike the claimed interconnect structures.

As noted above, Suemura et al has not recognized, taught or suggested to one of skill in the art the desirability of multi-level, modular, interconnect structures as claimed for the purpose of bringing regularity and order to circumstances where numerous signal outputs need to be coupled to numerous signal inputs without any transformations or signal processing. Hence, for all of the above reasons, the pending claims including the newly added claims are allowable, and such allowance is respectfully requested.

Additionally, the Examiner's attention is drawn to the attached copy of an Information Disclosure Statement and prior art documents which were submitted at the filing of the present application. Those documents, which were noted on the return receipt post card, copy enclosed,

were apparently lost and not referred to in the summary sheet of the Office Action. It is requested that the enclosed documents be considered and made of record in connection with this application. In view of the fact that the enclosed Disclosure Statement was submitted to the Patent Office when the application was filed, no fee should be necessary at this time.

A marked copy of the claims as amended is attached.

Respectfully submitted,

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Marked Copy Of Amended Claim

41. (Twice Amended) A signal coupling network for coupling any one of N1 inputs to any one of N2 outputs comprising:

a plurality, of substantially identical, [static,] KxK signal interconnect modules wherein each contains K^2 input lines, where K<N1, and couples them to K^2 output lines and wherein a separate signal path couples each input line to a respective output line of each module.

--63. (Amended) [A network as in claim 42] A signal coupling network for coupling any one of N1 inputs to any one of N2 outputs comprising:

a plurality of substantially identical, KxK signal interconnect modules wherein each contains K^2 input lines, where K<N1, and couples them to K^2 output lines wherein a separate signal path couples each input line to a respective output line of each module

wherein each KxK module [comprises:] includes:

a body portion which includes a plurality of LxL signal coupling networks with L<K;

K input ports coupled to the body portion;

K output ports coupled to the body portion; and

a plurality of signal paths, carried by the LxL signal coupling networks, the signal paths couple the input ports to the output ports.--

--66. (Amended) [A network as in claim 42] A signal coupling network for coupling any one of N1 inputs to any one of N2 outputs comprising:

a plurality of substantially identical, static, KxK signal interconnect modules wherein each contains K^2 input lines, where K<N1, and couples them to K^2 output lines;

wherein N1 inputs comprise $\frac{N1}{K}$ groups of signal carriers coupled to a corresponding number of KxK modules.